2011 VLSI Technology Short Course Program

“Logic & Memory towards 15 nm node - Technology and Circuit Design Co-optimization -”

Monday, June 13, 2011 (Shunju I)

Organizers/Chairs: Satoshi Inaba, *Toshiba Corp*.
Mukesh V. Khare, *IBM Corp.*

8:05	**Welcome Address and Introduction**
8:15	**CMOS Device Technologies for SoC** Rama Divakaruni, *IBM Corp.*
9:25	**Technology and Design Interaction at 20 nm and Beyond** Richard Klein, *AMD*
10:35	**Break**
10:50	**SRAM and Embedded Memories** Ping-Wei Wang, *TSMC*
12:00	**Lunch**
13:30	**Device Characteristics Variability and RTN** Kiyoshi Takeuchi, *Renesas Electronics Corp.*
14:40	**Break**
14:55	**DRAM and Future Commodity Memories** Seon Yong Cha, *Hynix Semiconductor Inc.*
16:05	**3D-IC Design Technologies** Durodami Lisk, *Qualcomm Inc.*
17:15	**Conclusion**

(as of May 18, 2011)